IN THE UNITED STATES DISTRICT COURT

FOR THE WESTERN DISTRICT OF TEXAS

WACO DIVISION

DEMARAY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:20-cv-00634

JURY TRIAL DEMANDED

DEMARAY LLC'S COMPLAINT FOR INFRINGEMENT OF U.S. PATENT NOS. 7,544,276 AND 7,381,657

Plaintiff Demaray LLC ("Demaray"), by and through its undersigned counsel, pleads the following against Intel Corporation ("Intel") and alleges as follows:

THE PARTIES

1. Dr. Richard Ernest Demaray, a named inventor on both of the patents at issue in this case, has been working in and with the semiconductor industry for more than forty years. Dr. Demaray began his training in chemical physics, studying ultraviolet photoconductivity of materials. His doctoral work focused on cross-supersonic molecular and atomic beams with which he demonstrated lossless conversion of molecular vibration to light in vacuum. During his post-doctoral fellowship, he designed and built some of the first pulsed xcimer laser driven tunable dye lasers for resonant multiphoton photoionization in the cooled beam. That work became instrumental to understanding the photo-physics of the high lying states of small and aromatic molecules.

2. Much of Dr. Demaray's work in industry has involved advances in thin film technology. In the 1980s, he worked as a senior physicist at BOC Group on electron beam evaporation technology used to deposit thermal barrier coatings. His work on adherent electron beam evaporation thermal barrier coatings revolutionized high-temperature jet engine performance, efficiency and longevity. Dr. Demaray's zirconia coatings are in worldwide production today on military, commercial and power generation turbine hot section blades and vanes. Later that decade and continuing into the early 1990s, Dr. Demaray worked at Varian Associates. He served as Varian's R&D Director for thin film systems, and developed full-face erosion and sputter physical vapor deposition technology now used extensively in semiconductor manufacturing worldwide. In the late 1990s, he helped form Applied Komatsu, where he served as General Manager of the PVD division and developed wide-area magnetron sputter machines. Thereafter, he managed several additional companies in the thin film space, including Symmorphix Inc., where he served as Chief Technology Officer and Chairman of the Board.

3. After serving in senior management roles at some of the more prominent companies in the industry, he founded Demaray in order to focus on research, development, and commercialization of new product applications based on technologies he had developed, including technologies protected by the patents at issue in this case. Much of that work—which remains ongoing—relates to the production of low-defect thin films for advanced electronic devices. In the course of his work, Dr. Demaray discovered that his patented technology was being used by Intel, without authorization, to manufacture thin films in Intel electronic devices with which Intel is generating many tens of billions of dollars per year.

4. Demaray is a Delaware limited liability company duly organized and existing under the laws of the State of Delaware. The address of the registered office of Demaray is 9 East

Loockerman Street, Suite 202, Dover, DE 19901. The name of Demaray's registered agent at that address is Spiegel & Utrera, P.A.

5. Demaray is the assignee and owns all right, title, and interest to U.S. Patent Nos. 7,544,276 ("the '276 Patent") and 7,381,657 ("the '657 Patent") (collectively, the "Asserted Patents"). A true and correct copy of the '276 Patent is attached hereto as Exhibit 1. A true and correct copy of the '657 Patent is attached hereto as Exhibit 2.

6. On information and belief, Defendant Intel is a corporation duly organized and existing under the laws of the State of Delaware, having a regular and established place of business in the Western District of Texas, including at 1300 South Mopac Expressway, Austin, Texas 78746.[1]

JURISDICTION AND VENUE

7. This is an action arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

8. Intel is subject to this Court's specific and general personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

9. Personal jurisdiction exists generally over Intel because Intel has sufficient minimum contacts with the forum as a result of business conducted within the State of Texas and the Western District of Texas and/or has engaged in continuous and systematic activities in the Western District of Texas, and Intel is registered with the Secretary of State to do business in the State of Texas. Personal jurisdiction also exists over Intel because it makes, uses, sells, offers for

[1] https://www.intel.com/content/www/us/en/location/usa.html; https://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html.

sale, imports, advertises, makes available, and/or markets products or processes within the State of Texas and the Western District of Texas that infringe one or more claims of the Asserted Patents, as alleged more particularly below.

10. Venue in this District is proper under 28 U.S.C. §§ 1400(b) and 1391(b) and (c) because Intel is subject to personal jurisdiction in this District and has committed acts of infringement in this District. Intel makes, uses, sells, and/or offers to sell infringing products or processes within this District, has a continuing presence within the District, and has the requisite minimum contacts with the District such that this venue is a fair and reasonable one. Upon information and belief, Intel has transacted, and at the time of the filing of the Complaint, is continuing to transact business within this District.

TECHNOLOGY BACKGROUND

11. Semiconductor devices are generally manufactured using a series of process steps applied to a substrate. A particularly important portion of typical semiconductor manufacturing processes involves the deposition of thin films used to form structures in the final product. One of the most practical and effective approaches to thin film deposition used to make modern semiconductor devices, and which is often used a dozen or more times in manufacturing even a single semiconductor product, is called "magnetron sputtering."

12. Magnetron sputtering is a physical vapor deposition ("PVD") technique. It can be carried out in a reactor that applies power to a target, *e.g.,* a metal such as tantalum (Ta) or titanium (Ti), to deposit a thin film onto a substrate, *e.g.,* silicon.

13. Magnetron sputtering, as practiced in modern commercial operations, generally involves the use of magnets behind the negative cathode in the reactor to create magnetic and electrical fields superimposed on the metal target. *See also, e.g.,* Ex. 1 at 8:38-60. An inert gas,

e.g., argon, can be introduced into the chamber to create a magnetically confined ionized plasma. The plasma may be located near the surface of the metal target such that the positively charged plasma ions collide with the negatively charged metal target material ejecting atoms from the metal target, which then deposit on the substrate. *See also, e.g., id.* at 5:24-27.

14. One form of magnetron sputtering is bias pulsed DC ("BPDC") sputtering. As that process is practiced in semiconductor industry today, a DC power supply that provides alternating negative and positive voltages is generally applied to the metal target while an RF voltage is generally applied to the substrate. *See also, e.g., id.* at 2:45-3:7, 5:60-67.

15. Reactive magnetron sputtering ("RMS"), as used currently for industrial scale semiconductor fabrication, generally includes the addition of a reactive gas, *e.g.,* nitrogen, as a process gas while sputtering from a metal target. *See also, e.g., id.* at 8:61-67. As an example, RMS using nitrogen gas can be used for depositing dielectric barrier layers of tantalum nitride (TaN) or titanium nitride (TiN) for copper interconnects on silicon wafers for semiconductor devices. BPDC sputtering systems are now being used for RMS sputtering.

FIRST CLAIM

(Infringement of U.S. Patent No. 7,544,276)

16. Demaray re-alleges and incorporates herein by reference Paragraphs 1-15 of its Complaint.

17. The '276 Patent, entitled "Biased pulse DC reactive sputtering of oxide films," was duly and lawfully issued on June 9, 2009. Ex. 1.

18. The '276 Patent names Hongmei Zhang, Mukundan Narasimhan, Ravi B. Mullapudi, and Richard E. Demaray as co-inventors.

19. The ’276 Patent has been in full force and effect since its issuance. Demaray owns by assignment the entire right, title, and interest in and to the ’276 Patent, including the right to seek damages for past, current, and future infringement thereof.

20. The ’276 Patent relates generally to a configuration of a reactor for deposition of thin films “by pulsed DC reactive sputtering,” which, in certain implementations, uses “a pulsed DC power supply providing alternating negative and positive voltages to the target” and “a narrow band-rejection filter” coupled between the pulsed DC power supply and a target area that receives a metal target to provide high quality deposition layers. *See, e.g.,* Ex. 1 at 1:12-14.

21. The ’276 Patent also describes, among other things, “a substrate electrode coupled to an RF power supply. A substrate mounted on the substrate electrode is therefore supplied with a bias from the RF power supply.” *Id.* at 2:45-53.

22. Demaray is informed and believes, and thereon alleges, that Intel has infringed, and unless enjoined will continue to infringe, one or more claims of the ’276 Patent, in violation of 35 U.S.C. § 271, by, among other things, (1) making, using, offering to sell, and selling within the United States, supplying or causing to be supplied in or from the United States, and/or importing into the United States, without authority or license, semiconductor manufacturing equipment including reactive magnetron sputtering reactors configured as described in the claims of the ’276 Patent; and/or (2) supplying or causing to be supplied in or from the United States (a) all or a substantial portion of the components of semiconductor manufacturing equipment including reactive magnetron sputtering reactors configured as described in the claims of the ’276 Patent in such manner as to actively induce the combination of such components outside of the United States in a manner that would infringe the ’276 Patent if such combination occurred within the United States, and/or (b) a component of semiconductor manufacturing equipment including reactive

magnetron sputtering reactors configured as described in the claims of the '276 Patent that is especially made or especially adapted for use in the invention and not a staple article or commodity of commerce suitable for substantial noninfringing use, where such component is uncombined in whole or in part, and Intel knows that such component is so made or adapted and intends that such component will be combined outside of the United States in a manner that would infringe the '276 patent if such combination occurred within the United States.

23. For example, the accused products for the '276 Patent embody every limitation of claims of the '276 Patent, literally or under the doctrine of equivalents, including as set forth in the illustrative example below. The further descriptions below are preliminary examples and are non-limiting.

["1. A reactor according to the present invention, comprising:"]

24. On information and belief, Intel uses infringing RMS reactors ("Intel RMS reactors") according to the claims of the '276 Patent in the production of its semiconductor products at its semiconductor fabrication plants and research facilities, including but not limited to premises within the United States.

25. As an example, on information and belief, Intel configures RMS reactors, including, but not limited to reactors in the Endura product line from Applied Materials, Inc. ("Applied Materials") for deposition of layers (including, *e.g.*, metal nitride layers, such as, for instance, TaN barrier layers and/or TiN hardmask layers) in its semiconductor products. Intel has identified Applied Materials as a Preferred Quality Supplier.[2] On information and belief, these reactors can be modified with application-specific process kits to deposit specific materials. The

[2] http://www.appliedmaterials.com/company/news/press-releases/2019/03/applied-materials-receives-intel%E2%80%99s-preferred-quality-supplier-award.

Endura product line includes reactors that can be configured for deposition of TaN layers (*e.g.,* CuBS RFX PVD with the Encore II Ta(N) barrier chamber) and TiN layers (*e.g.,* Cirrus ionized PVD chamber). A true and correct copy of a brochure for the Endura product line is attached as Exhibit 3. A true and correct copy of an article from the Nanochip Technical Journal regarding TaN deposition chambers is attached as Exhibit 4.[3] A true and correct copy of a presentation on the Cirrus TiN deposition chambers is attached as Exhibit 5.[4] An example image of an Endura CuBS RFX PVD is shown below:[5]

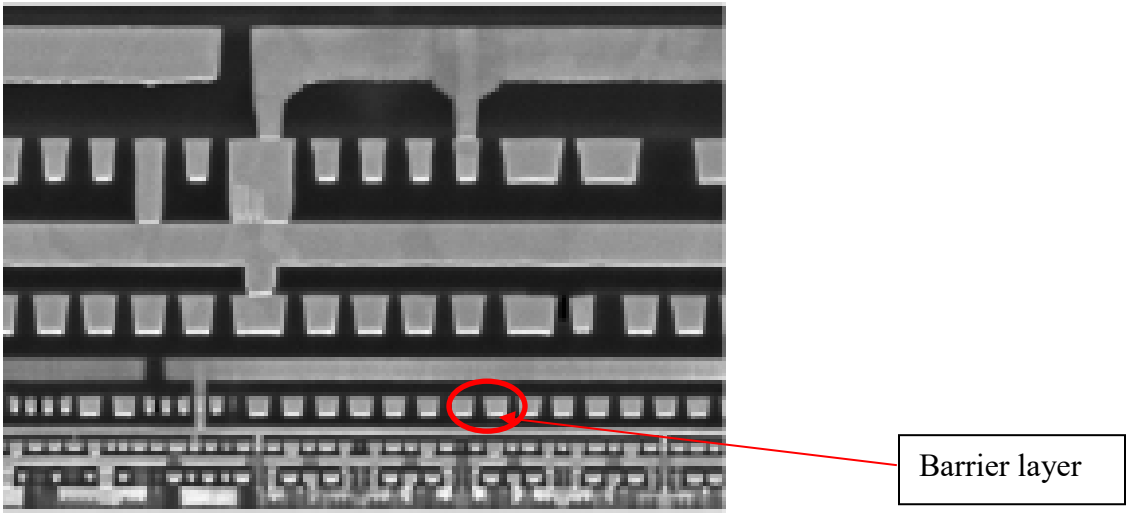
26. As an example, on information and belief, Intel has configured, or causes to be configured, and uses and/or has used infringing Intel RMS reactors for TaN barrier layer deposition with its copper interconnects in the fabrication of its processors, including but not limited to its Broadwell Processors. On information and belief, for example, Intel has configured, or causes to

[3] https://www.appliedmaterials.com/files/nanochip-journals/nanochiptechjournal_vol6_issue2.pdf#page=45.

[4] http://www.appliedmaterials.com/files/pdf_documents/cirrus_htx_pvd_techncial_briefing.pdf.

[5] http://www.appliedmaterials.com/products/endura-cubs-rfx-pvd.

be configured, and uses infringing Intel RMS reactors in the fabrication of TaN barrier layers in its Core M 5Y70/5Y10 14nm Gen 2 Broadwell Processors. An example of copper interconnects with metal nitride barrier layers in Intel 14nm Broadwell Processors is shown below:[6]



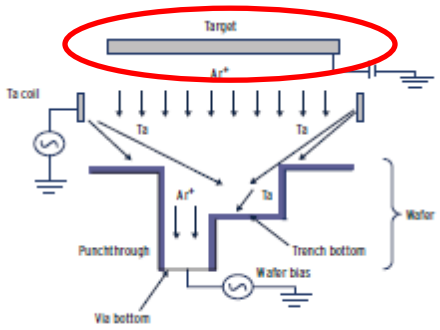
["a target area for receiving a target;"]

27. The Intel RMS reactors comprise a target area for receiving a target.

28. For example, for Intel RMS reactors, "[i]n PVD, the target is the source of the material to be deposited. Atoms are ejected from the target as a result of the bombardment of energetic particles."[7] In Intel RMS reactors for depositing TaN, tantalum is the source material (*i.e.,* the metal target). *See* Ex. 3 at 4 (Cu barrier reactor for TaN). The reactors include a target area (indicated as "target" in the image below) for receiving the tantalum:

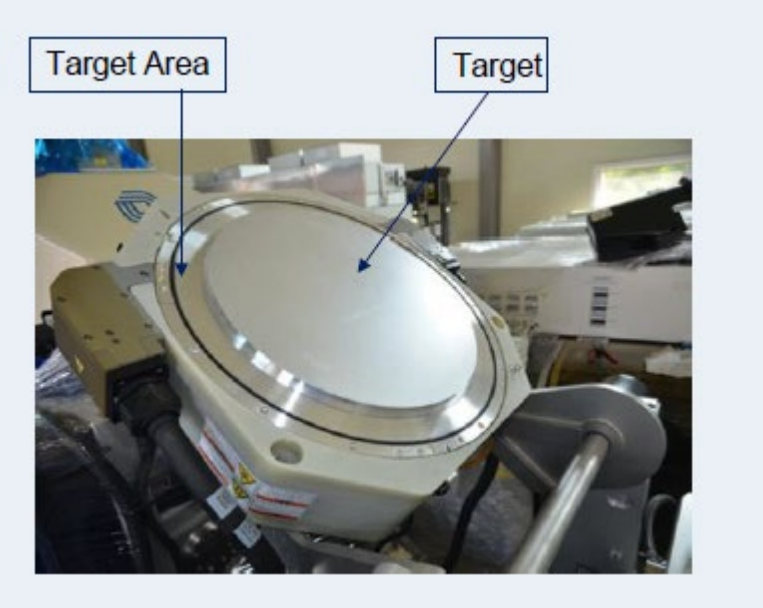
[6] https://www.intel.com/content/dam/www/public/us/en/documents/technology-briefs/bohr-14nm-idf-2014-brief.pdf.

[7] https://www.appliedmaterials.com/resources/glossary.



Ex. 4 at 42 (Fig. 1).

29. An example of the target and target area in a RMS reactor is shown below:



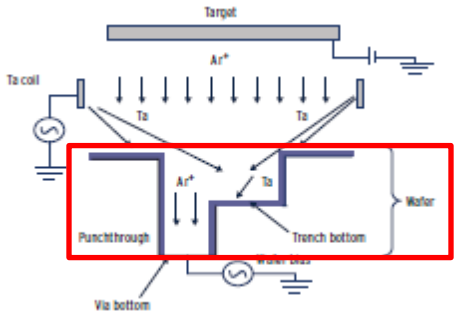
["a substrate area opposite the target area for receiving a substrate;"]

30. The Intel RMS reactors comprise a substrate area opposite the target area for receiving a substrate.

31. For example, for Intel RMS reactors a substrate is "[t]he material upon which thin films are manipulated. Silicon is most commonly used for semiconductors …."[8] The substrate in a RMS reactor for deposition of a TaN barrier layer in the Broadwell Processors, for instance, is a

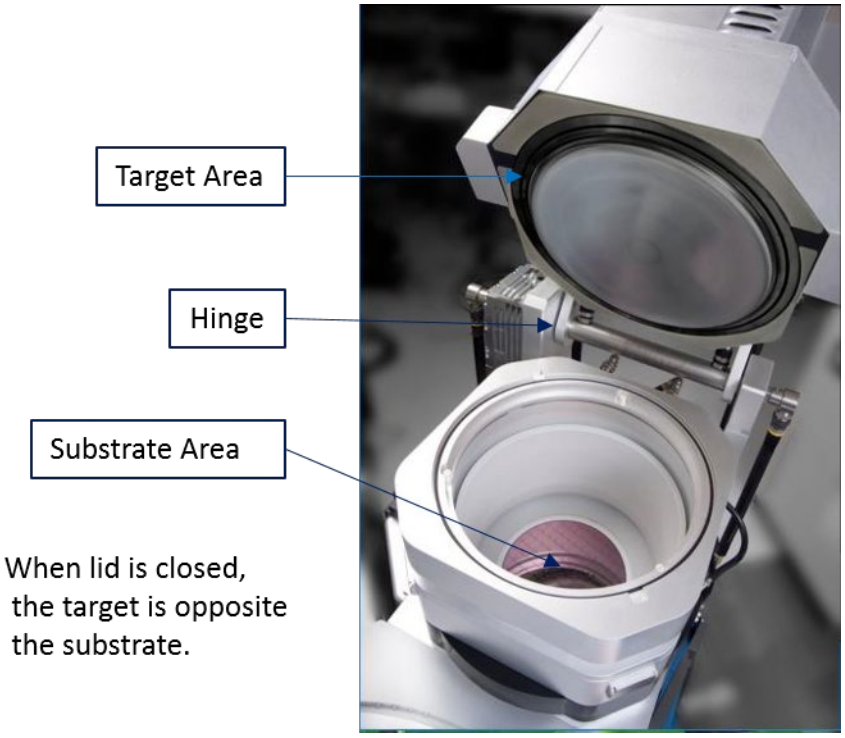
[8] https://www.appliedmaterials.com/resources/glossary.

silicon wafer. A substrate area is opposite the target area for receiving the silicon substrates (indicated as "wafer") as illustrated below:



See Ex. 4 at 42 (Fig. 1).

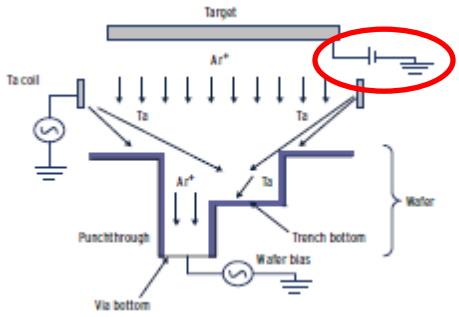
32. The substrate area in a RMS reactor is shown below:



["a pulsed DC power supply coupled to the target area, the pulsed DC power supply providing alternating negative and positive voltages to the target;"]

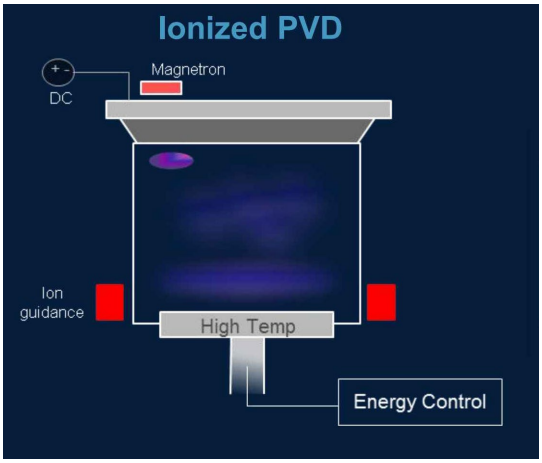
33. On information and belief, Intel configures, or causes to be configured, the Intel RMS reactors such that they comprise a pulsed DC power supply coupled to the target area, and the pulsed DC power supply provides alternating negative and positive voltages to the target.

34. For example, on information and belief, in the Intel RMS reactors a power source is coupled to the target area as illustrated below:

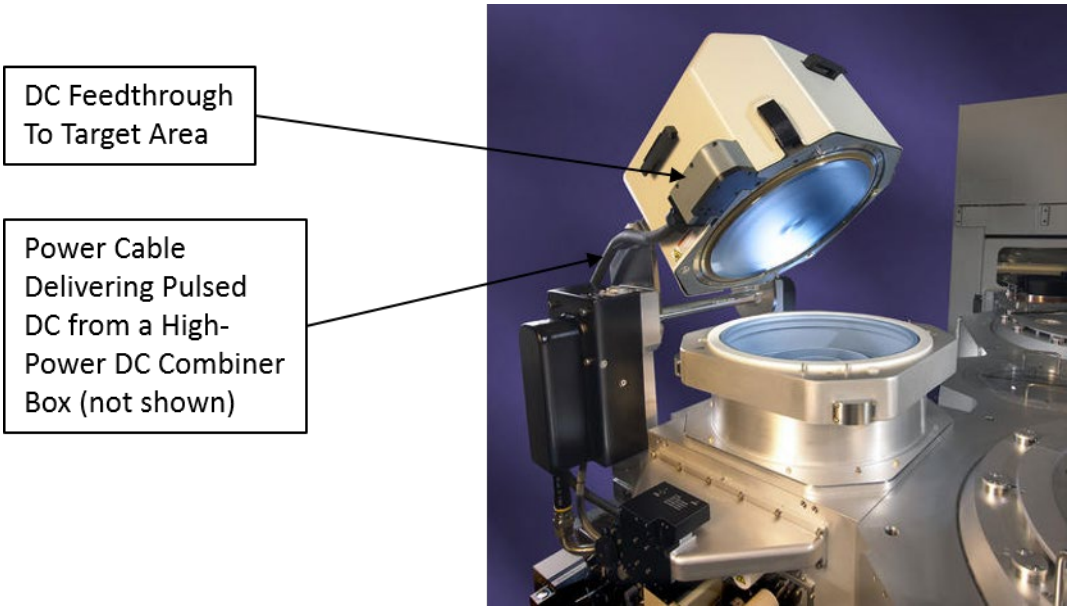


See Ex. 4 at 42 (Fig. 1).

35. The presence of a DC power unit in a reactor for RMS deposition (*e.g.*, TaN when using a tantalum target and a process gas that includes nitrogen) is illustrated below:



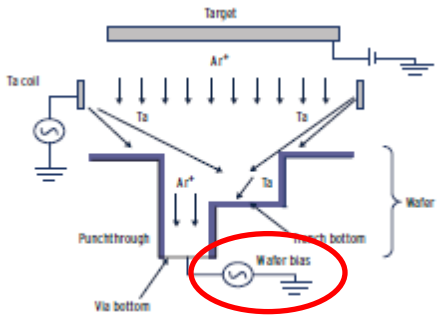
See Ex. 5 at 9 ("DC" power supply in 1st generation iPVD products). The presence of a pulsed DC power unit in a reactor configured for RMS deposition (*e.g.,* TaN, when using a tantalum target and a process gas that includes nitrogen) is shown below:



["an RF bias power supply coupled to the substrate;"]

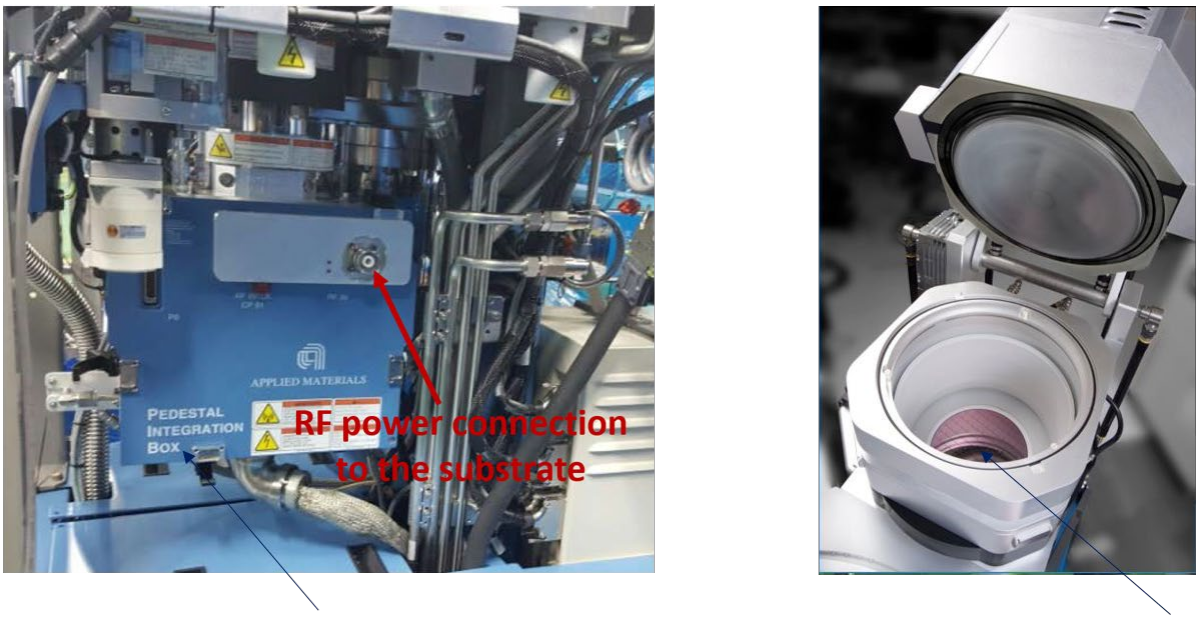
36. On information and belief, Intel configures, or causes to be configured, the Intel RMS reactors such that they comprise an RF bias power supply coupled to the substrate.

37. For example, a power supply is coupled to the substrate area to bias the substrate as illustrated below:



See Ex. 4 at 42 (Fig. 1).

38. The presence of an RF bias power supply in a reactor for RMS deposition (*e.g.*, TaN, when using a tantalum target and a process gas that includes nitrogen) is shown below:



The Pedestal Integration Box (PIB) couples the RF bias power supply to the substrate (not shown) via the substrate area

["and a narrow band-rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.]

39. On information and belief, Intel configures, or causes to be configured, the Intel RMS reactors such that they comprise a narrow band-rejection filter that rejects at a frequency of the RF bias power supply coupled between the pulsed DC power supply and the target area.

40. On information and belief, a narrowband filter is coupled between the pulsed DC power supply and the target area in a reactor for deposition of tantalum nitride (when using a tantalum target and a process gas that includes nitrogen). On information and belief, a narrowband filter is used in the Intel RMS reactors as configured to, for example, protect the pulsed DC power supply from feedback from the RF bias power supply.

SECOND CLAIM

(Infringement of U.S. Patent No. 7,381,657)

41. Demaray re-alleges and incorporates herein by reference Paragraphs 1-40 of its Complaint.

42. The ’657 Patent, entitled “Biased pulse DC reactive sputtering of oxide films,” was duly and lawfully issued on June 3, 2008. Ex. 2.

43. The ’657 Patent names Hongmei Zhang, Mukundan Narasimhan, Ravi B. Mullapudi, and Richard E. Demaray as co-inventors.

44. The ’657 Patent has been in full force and effect since its issuance. Demaray owns by assignment the entire right, title, and interest in and to the ’657 Patent, including the right to seek damages for past, current, and future infringement thereof.

45. The ’657 Patent generally relates to a method of depositing thin films “by pulsed DC reactive sputtering.” Ex. 2 at 1:11-13.

46. The ’657 Patent describes, among other things, methods of using a “sputtering reactor according to the present invention includes a pulsed DC power supply coupled through a filter to a target and a substrate electrode coupled to an RF power supply. A substrate mounted on the substrate electrode is therefore supplied with a bias from the RF power supply.” *Id.* at 2:45-54.

47. Demaray is informed and believes, and thereon alleges, that Intel has infringed and unless enjoined will continue to infringe one or more claims of the ’657 Patent, in violation of 35 U.S.C. § 271, by, among other things, using the claimed methods for reactive sputtering in an infringing manner to produce semiconductor products, and/or making, offering to sell, and selling within the United States, and/or importing into the United States, without authority or license,

semiconductor products produced using the claimed methods for reactive sputtering in an infringing manner.

48. For example, the accused products for the '657 Patent are produced by a method that embodies every limitation of claims of the '657 Patent, literally or under the doctrine of equivalents, including as set forth in the illustrative example below. The further descriptions below are preliminary examples and are non-limiting.

["A method of depositing a film on an insulating substrate, comprising:"]

49. On information and belief, Intel uses a method of depositing a film on an insulating substrate according to the claims of the '657 Patent in the production of semiconductor products at its semiconductor fabrication plants and research facilities, including but not limited to its premises within the United States.

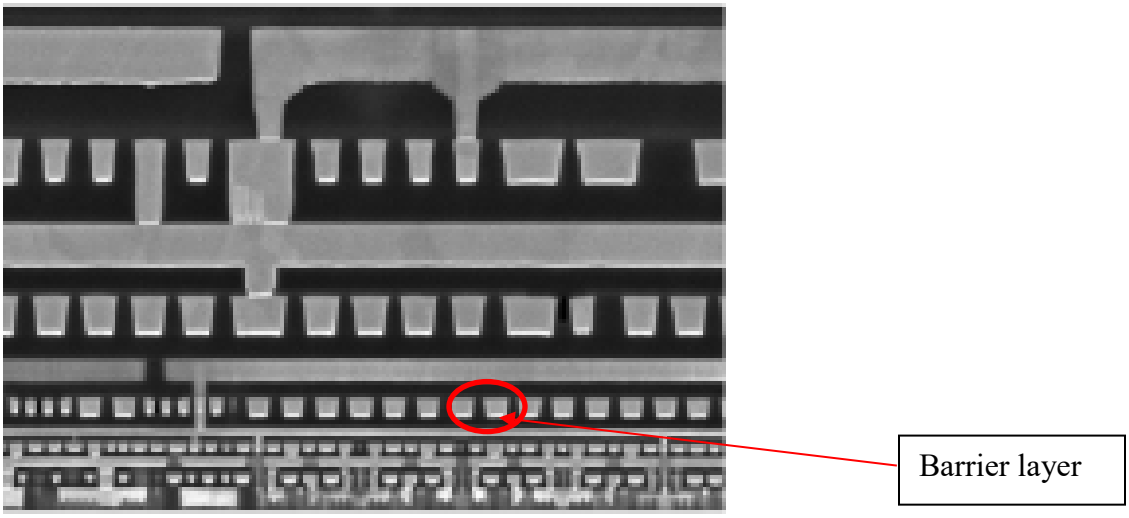
50. As an example, on information and belief, Intel deposits layers (including, *e.g.*, metal nitride layers such as, for instance, TaN barrier layers and/or TiN hardmask layers) on insulating substrates (*e.g.*, semiconductor wafers) for its processors, including but not limited to its Broadwell Processors.

["providing a process gas between a conductive target and the substrate;"]

51. On information and belief, Intel fabricates semiconductor products using a method comprising providing a process gas between a conductive target and the substrate.

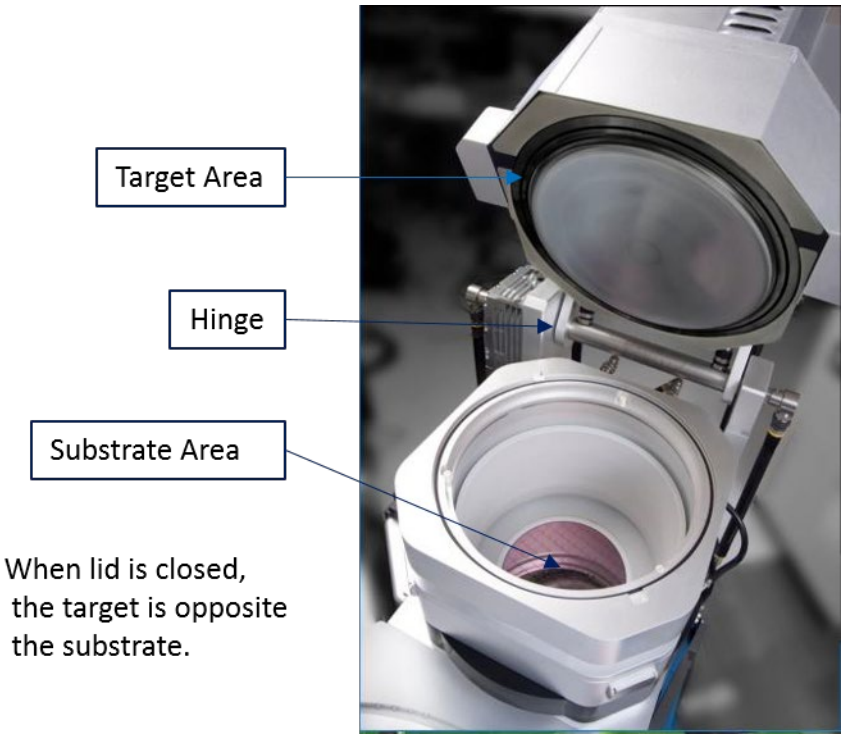
52. As an example, on information and belief, for example, Intel uses a RMS reactor in the fabrication of TaN barrier layers in its Core M 5Y70/5Y10 14nm Gen 2 Broadwell Processors. On information and belief, Intel uses a RMS reactor that it configures to use with nitrogen as a process gas. *See also, e.g.,* Ex. 3 at 6. The constitution of the metal nitride barrier

layers confirms the use of nitrogen as a process gas. Copper interconnects with metal nitride barrier layers in Intel 14nm Broadwell Processors are shown below:[9]



53. On information and belief, in RMS reactors as configured, a process gas including nitrogen (*e.g.*, N_2 or NH_3) is provided in the chamber between the tantalum target and the silicon substrate to deposit a tantalum nitride (TaN) film on the substrate. For example, the presence of a process chamber between a conductive target and the substrate (*e.g.*, TaN, when using a tantalum target and a process gas that includes nitrogen) is shown below:

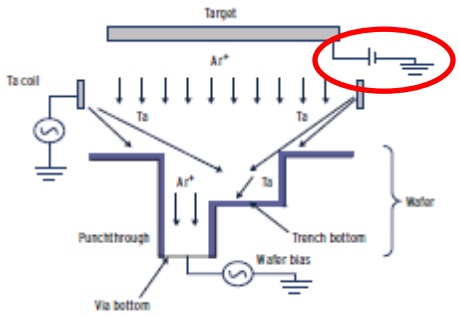
[9] https://www.intel.com/content/dam/www/public/us/en/documents/technology-briefs/bohr-14nm-idf-2014-brief.pdf.



["providing pulsed DC power to the target through a narrow band rejection filter such that the target alternates between positive and negative voltages;"]

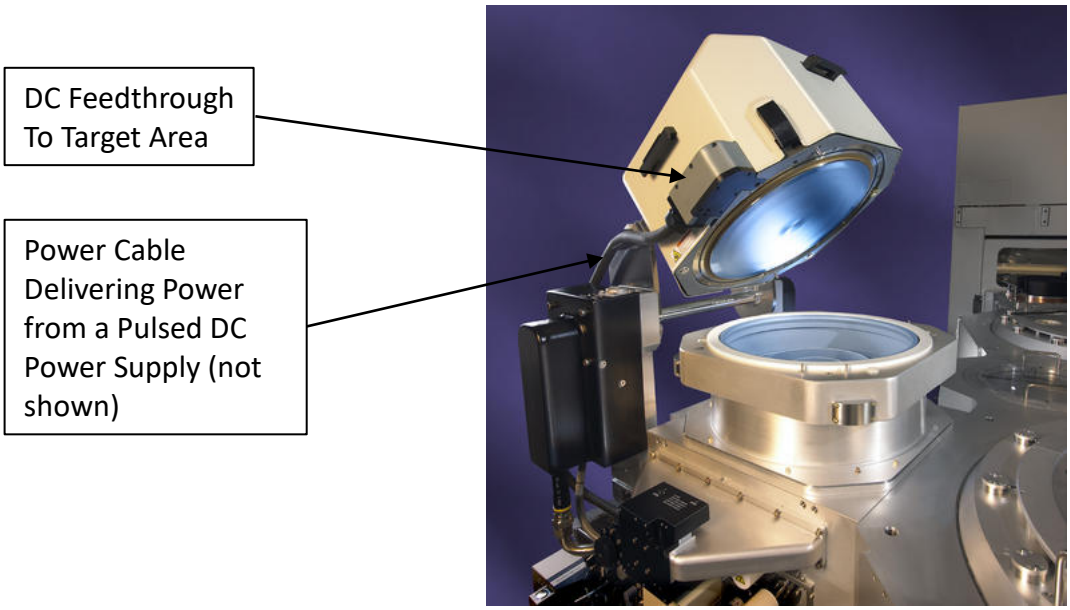
54. On information and belief, Intel fabricates semiconductor products using a method comprising providing pulsed DC power to the target through a narrow band rejection filter such that the target alternates between positive and negative voltages.

55. As an example, as discussed above, on information and belief, Intel uses a RMS reactor in the fabrication of TaN barrier layers in its semiconductor products, including, for example, the Broadwell Processors. *See also, e.g.,* Ex. 3 at 6. A power source is coupled to the target as illustrated below:



See Ex. 4 at 42 (Fig. 1).

56. The presence of a pulsed DC power unit in a reactor configured for RMS deposition (*e.g.*, TaN, when using a tantalum target and a process gas that includes nitrogen) is shown below:

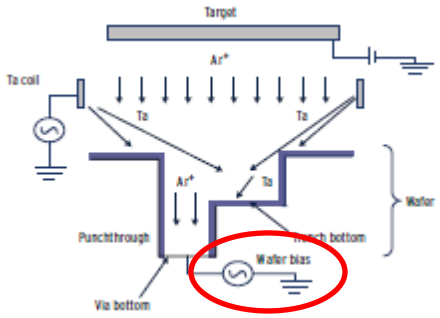


57. On information and belief, a narrowband filter is coupled between the pulsed DC power supply and the target area in a reactor for deposition of, *e.g.*, TaN, when using a tantalum target and a process gas that includes nitrogen. On information and belief, a narrowband filter is used in the Intel RMS reactors as configured to, for example, protect the pulsed DC power supply from feedback from the RF bias power supply.

["providing an RF bias at a frequency that corresponds to the narrow band rejection filter to the substrate;"]

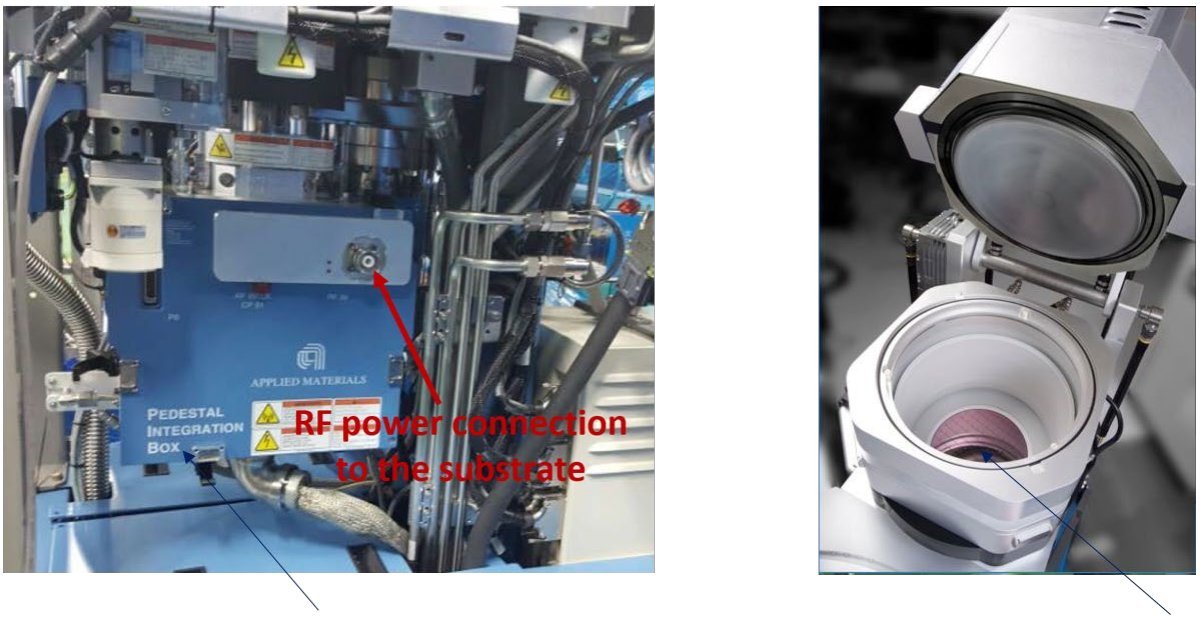
58. On information and belief, Intel fabricates semiconductor products using a method comprising providing an RF bias at a frequency that corresponds to the narrow band rejection filter to the substrate.

59. As an example, as discussed above, on information and belief, Intel uses a RMS reactor in the fabrication of TaN barrier layers in its semiconductor products, including, for example, the Broadwell Processors. *See also, e.g.,* Ex. 3 at 6. An RF power supply is coupled to the substrate area to bias the substrate as illustrated below:



See Ex. 4 at 42 (Fig. 1).

60. The presence of an RF bias power supply in a reactor configured for RMS deposition (*e.g.*, TaN, when using a tantalum target and a process gas that includes nitrogen) is shown below :



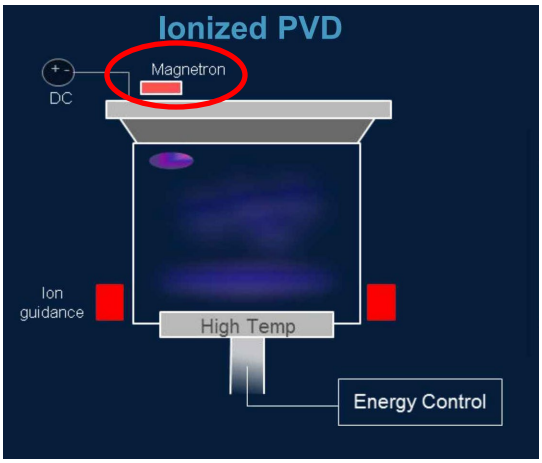
The Pedestal Integration Box (PIB) couples the RF bias power supply to the substrate (not shown) via the substrate area

["providing a magnetic field to the target;"]

61. On information and belief, Intel fabricates semiconductor products using a method comprising providing a magnetic field to the target.

62. As an example, as discussed above, on information and belief, Intel uses a RMS reactor in the fabrication of barrier layers, *e.g.*, TaN (when using a tantalum target and a process gas that includes nitrogen), in its semiconductor products, including, for example, the Broadwell Processors. *See also, e.g.,* Ex. 3 at 6. As configured in the Intel RMS reactors, RMS involves the use of magnets to provide a magnetic field to the target.

63. The presence of a magnetron in a reactor for deposition of tantalum nitride (when using a tantalum target and a process gas that includes nitrogen) is illustrated below. *See* Ex. 5 at 9 (1st generation iPVD products):



[“and reconditioning the target;”]

64. On information and belief, Intel fabricates semiconductor products using a method comprising reconditioning the target.

65. As an example, as discussed above, on information and belief, Intel uses a RMS reactor in the fabrication of TaN barrier layers in its semiconductor products, including, for example, the Broadwell Processors. *See also, e.g.,* Ex. 3 at 6. On information and belief, as configured in the Intel RMS reactors with nitrogen process gas, impurities, such as nitrides, generated in the deposition process are removed from the tantalum target surface prior to the next deposition by sputtering in the absence of the nitrogen process gas.

[“wherein reconditioning the target includes reactive sputtering in the metallic mode and then reactive sputtering in the poison mode.”]

66. On information and belief, Intel fabricates semiconductor products using a method in which the reconditioning of the target includes reactive sputtering in the metallic mode and then reactive sputtering in the poison mode.

67. As an example, as discussed above, on information and belief, Intel uses a RMS reactor in the fabrication of TaN barrier layers in its semiconductor products, including, for example, the Broadwell Processors. *See also, e.g.,* Ex. 3 at 6. On information and belief, as

configured in the Intel RMS reactors with nitrogen process gas, impurities, such as nitrides, generated in the deposition process are removed from the tantalum target surface prior to the next deposition by sputtering in the absence of the nitrogen process gas before the next deposition by sputtering in the presence of nitrogen.

68. Intel has had knowledge of the Asserted Patents and its infringement thereof at least as of the filing of this Complaint.

69. As a result of Intel's infringement of the Asserted Patents, Demaray has been damaged. Demaray is entitled to recover for damages sustained as a result of Intel's wrongful acts in an amount subject to proof at trial.

70. In addition, Intel's infringing acts and practices have caused, are causing, and unless enjoined will continue to cause immediate and irreparable harm to Demaray.

71. To the extent 35 U.S.C. § 287 is determined to be applicable, on information and belief its requirements have been satisfied with respect to the Asserted Patents.

PRAYER FOR RELIEF

WHEREFORE, Demaray prays for judgment against Intel as follows:

A. That each of the Asserted Patents is valid and enforceable;

B. That Intel has infringed, and unless enjoined will continue to infringe, each of the Asserted Patents;

C. That Intel pay Demaray damages adequate to compensate Demaray for Intel's infringement of each of the Asserted Patents, together with interest and costs under 35 U.S.C. § 284;

D. That Intel be ordered to pay prejudgment and post-judgment interest on the damages assessed;

E. That Intel be ordered to pay supplemental damages to Demaray, including interest, with an accounting, as needed;

F. That Intel be enjoined from infringing the Asserted Patents, or if its infringement is not enjoined, that Intel be ordered to pay ongoing royalties to Demaray for any post-judgment infringement of the Asserted Patents;

G. That this is an exceptional case under 35 U.S.C. § 285, and that Intel pay Demaray's attorneys' fees and costs in this action; and

H. That Demaray be awarded such other and further relief, including equitable relief, as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Federal Rule of Civil Procedure 38(b), Demaray hereby demands a trial by jury on all issues triable to a jury.

Dated: July 14, 2020

Morgan Chu (*pro hac vice*)
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